WHAT IS CLAIMED IS:

1. A limiting circuit for a brushless dc motor, comprising:

a first transistor and a second transistor arranged in complementary connection, the first transistor connected to a motor drive circuit and regarded as a first switch, and the second transistor regarded as a second switch and adapted to control the first transistor;

a first resistor provided with a first bias for the first switch to thereby turn on or off the motor drive circuit; and

a second resistor provided with a second bias for the second switch to thereby turn on or off the first switch;

wherein when an electric current supplied from a power source is risen rapidly, the second switch is turned on so that the first switch is turned off to thereby cut off the motor drive circuit from the power source; and

wherein the first switch and the second switch are operated alternatively until the electric current of the power source is stable.

2. The limiting circuit for a brushless dc motor as defined in Claim 1, wherein the transistors are NPN type transistors.

3. The limiting circuit for a brushless dc motor as defined in Claim 1, wherein the transistors are P type field-effect transistors.

4. The limiting circuit for a brushless dc motor as defined in Claim 1,

13

wherein the transistors are PNP type transistors.

5. The limiting circuit for a brushless dc motor as defined in Claim 1, wherein the transistors are N type field-effect transistors.

6. The limiting circuit for a brushless dc motor as defined in Claim 1, wherein the limiting circuit has a first terminal connected to the power source, and a second terminal connected to the motor drive circuit, the first terminal is formed with an end of the first resistor and the second terminal formed with an end of the first switch.

7. The limiting circuit for a brushless dc motor as defined in Claim 1, wherein the limiting circuit has a first terminal connected to the power source, and a second terminal connected to the motor drive circuit, the first terminal is formed with an end of the second switch and the second terminal formed with an end of the first switch.